

08/902133

DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY
MEMORY AND METHODS OF FABRICATION AND USE

Abstract of the Disclosure

5 A floating gate transistor has a reduced barrier energy at an interface with an adjacent gate insulator, allowing faster charge transfer across the gate insulator at lower voltages. Data is stored as charge on the floating gate. The data charge retention time on the floating gate is reduced. The data stored on the floating gate is dynamically refreshed. The floating gate transistor provides a dense and planar dynamic electrically
10 alterable and programmable read only memory (DEAPROM) cell adapted for uses such as for a dynamic random access memory (DRAM) or a dynamically refreshed flash EEPROM memory. The floating gate transistor provides a high gain memory cell and low voltage operation.

"Express Mail" mailing label number: EM031314260 US
Date of Deposit: July 29, 1997
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231
Printed Name Matthew Hollister
Signature [Signature]